REMARKS

Claims 1-14 stand rejected under 35 USC §103(a) as being unpatentable over Constantinescu, U.S. patent application US 2004/0252644 A1 in view of Schraff publication from Sensor Magazine Online, December 1997.

Claims 1, 8 and 14 have been amended to more clearly state the invention. Reconsideration and allowance of each of the pending claims 1-14, as amended, is respectfully requested.

Constantinescu, U.S. patent application US 2004/0252644 A1 discloses a receiver that can receive from an interconnect information packets and idle packets, where one or more of the idle packets includes a test pattern. A condition detector can detect a condition of the interconnect in response to the test pattern. Constantinescu states:

> [0021] Component 202 includes drivers 208, test pattern generator 210, encoder/decoder 212, and leaky bucket 214. Drivers 208 could include drivers using GTL (Gunning Transistor Logic), differential signaling drivers, and/or differential signaling drivers such as Low Voltage Differential Signaling Drivers (LVDs), for example. Test pattern generator 210 produces a test pattern which may be included in idle packets transmitted by component 202 via interconnect 206. According to some embodiments the test pattern produced by test pattern generator 210 may be a stress pattern selected to stress the interconnect more than regular information such as data and/or control transmitted via the interconnect. Encoding/decoding may be performed by encoder/decoder 212 using, for example, either cyclical redundancy check (CRC) or error correcting codes (ECC). Alternatively or in addition to CRC and/or ECC, errors within the idle packet may also be detected by checking the received packet against a known stress pattern. (Emphasis added)
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> [0028] After the information packet is sent at 308 a decision is made at 310 to determine if a transaction has successfully completed. Successful completion of a transaction may be confirmed, for example, by the return of data (such as in the case of read commands) or an acknowledge message (such as in the case of write commands). If a successful transaction has completed as determined at 310 flow can then return, for example, to check information queues at 302. However, if a successful

transaction has not completed as determined at 310, failed transactions may be retried, for a predefined number of times at 312 and 314. If a retry limit is exceeded at 312 a failed interconnect flag may be set at 316. If the retry limit is not exceeded at 312 the transaction may be retried at 314, after which a determination may be made at 310 again to see if the retried transaction is successful. After a failed interconnect flag is set at 316 when the retry limit is exceeded at 312, an error handling routine may be entered at 318. After error handling, control can be transferred to the system's Operating System (OS). The error handling routine entered at 318 attempts confinement of the errors induced by the failure. In this case the application or applications that initiated the uncompleted transaction or transactions have to be terminated. If the operating system is affected by the interconnect failure a system crash occurs. FIG. 4 illustrates a flow diagram 400 representing error detection and failure prediction at a receiver. This can help signal an interconnect failure and lead to avoidance of a crashed system, for example. The flow illustrated in FIG. 4 according to some embodiments may be implemented using, for example, a component such as any of those illustrated in other drawings herein (for example by any of the processors 102, switch 104, memory controllers 110 or I/O controllers 114 illustrated in FIG. 1 or any of the components 202 and 204 illustrated in FIG. 2 or by any other components illustrated herein in later FIGS.). However, the embodiments illustrated in FIG. 4 need not be limited to being performed by such components and need not perform exactly the same flow as illustrated in FIG. 4. Many variations of the flow illustrated in FIG. 4 may be implemented according to some embodiments. An example of where error detection and failure prediction of an interconnect failure may be implemented is in some embodiments using CRC.

[0032] If a failure is determined at 412 then a failure prediction flag is set at 414, for example, if a predefined number of errors are accumulated over a given period of time. After the failure prediction flag is set at 414 an error handling routine 416 may be used to start a process of isolating the interconnect. The interconnect may be isolated, for example, by notifying the operating system, activating a spare interconnect if one is available or finding a degraded configuration, querying the traffic over the interconnect, and/or disabling the drivers. The isolation process may be platform, firmware and operating system specific for a variety of different embodiments. Once the error handling routine 416 has finished control may be transferred to the operating system, for example. (Emphasis added)

The Schraff publication discloses a method for choosing differential or single-ended measurements for data acquisitions systems. Figure 1 illustrates a 4-channel multiplexer, sampled data system. Schraff discloses that the type of signal chosen to configure the system depends entirely on the application.

Applicants respectfully submit that each of the pending claims 1-14, as

amended, is patentable over the references of record, including Constantinescu and Schraff.

Independent claim 1, as amended, recites a method for implementing a redundancy enhanced differential signal interface. The recited method of the present invention includes the steps of providing a differential signaling I/O pair connected to a differential receiver interface; detecting an error from said differential receiver interface; responsive to said detected error, reducing an interface operating speed of said differential receiver interface; alternately testing of true and complement sides of a said differential signaling I/O pair; and responsive to detecting a failure of a true side or a complement side, setting the detected failed true side or complement side to a reference voltage and maintaining said reduced interface operating speed of said differential receiver interface.

The total teachings of Constantinescu as set forth above, fail to suggest the steps of providing a differential signaling I/O pair connected to a differential receiver interface; detecting an error from said differential receiver interface; responsive to said detected error, reducing an interface operating speed of said differential receiver interface. Schraff discloses configuring a system depending on the parameters of a particular application. Schraff adds nothing to suggest the step esponsive to said detected error, reducing an interface operating speed of said differential receiver interface, as taught and claimed by applicants. Neither one of Constantinescu and Schraff, and considering the total teachings in combination, suggest the step of responsive to detecting a failure of a true side or a complement side, setting the

detected failed true side or complement side to a reference voltage and maintaining said reduced interface operating speed of said differential receiver interface.

Applicants respectfully submit that Constantinescu and Schraff, considering the total teachings in combination, clearly fail to render obvious the claimed invention. Applicants respectfully submit that Constantinescu and Schraff, considering the total teachings in combination, fail to suggest the subject matter and the above recited steps of the present invention as set forth in independent claim 1, as amended. Thus, independent claim 1, as amended, is patentable.

Independent claim 8, as amended, recites apparatus for implementing a redundancy enhanced differential signal interface. The recited apparatus comprising a differential signaling I/O pair; a differential receiver interface coupled to said differential signaling I/O pair; said differential receiver interface including a pair of multiplexers coupled to a differential receiver, each multiplexer having a first input receiving a respective true or complement signal and a second input connected to a voltage reference and a multiplexer control input; and each multiplexer providing a respective true or complement output signal to said differential receiver; error detecting means coupled to said differential receiver interface for detecting an error; test and failure control logic coupled to said error detecting means and said differential receiver interface; said test and failure control logic being responsive to a detected error, for reducing an interface operating speed; and alternately enabling said multiplexer control input of said pair of multiplexers for testing of true and complement sides of said differential signaling I/O pair; and responsive to detecting a failure of a true side or a

complement side, for setting the detected failed true side or complement side of said differential receiver to a reference voltage for continued operation.

Applicants respectfully submit that claim 8 is patentable for reasons as set forth with respect to claim 1. Only applicants teach that when an error is detected, an interface operating speed is reduced in response to the detected error.

The total teachings of Constantinescu as set forth above in detail, fails to suggest error detecting means coupled to said differential receiver interface for detecting an error; test and failure control logic coupled to said error detecting means and said differential receiver interface; said test and failure control logic being responsive to a detected error, for reducing an interface operating speed; and alternately enabling said multiplexer control input of said pair of multiplexers for testing of true and complement sides of said differential signaling I/O pair; and responsive to detecting a failure of a true side or a complement side, for setting the detected failed true side or complement side of said differential receiver to a reference voltage for continued operation, as recited in independent claim 8, as amended. Schraff adds nothing to render obvious the subject matter of independent claim 8, as amended.

Applicants respectfully submit that Constantinescu and Schraff, considering the total teachings in combination, clearly fail to render obvious the claimed apparatus for implementing a redundancy enhanced differential signal interface as recited in independent claim 8, as amended. Thus, independent claim 8, as amended, is patentable.

Dependent claims 2-7, and 9-14 respectively depend from patentable

claims 1, and 8, further defining the invention. Each of the dependent claims 2-7, and 9-14, as amended, is likewise patentable.

Applicants have reviewed all the art of record, and respectfully submit that the claimed invention is patentable over all the art of record, including the references not relied upon by the Examiner for the rejection of the pending claims.

It is believed that the present application is now in condition for allowance and allowance of each of the pending claims 1-14, as amended, is respectfully requested. Prompt and favorable reconsideration is respectfully requested.

If the Examiner upon considering this amendment should find that a telephone interview would be helpful in expediting allowance of the present application, the Examiner is respectfully urged to call the applicants' attorney at the number listed below.

Respectfully submitted,

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